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Switched-capacitor multilevel inverter with self-voltage-balancing for high-frequency power distribution system

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Abstract: Switched capacitor multilevel inverter (SCMLI) with reduced components is attractive for higher number of voltage levels due to less implementation complexity and low cost. In this study, a new family of hybrid SCMLI for high frequency power distribution system is presented to eliminate the intermediate power conversion. Firstly, a five-level SCMLI employing a single voltage source is proposed, which is further extended to nine-level (9L) with its operation. Further extension/enhancement of the proposed 9L-SCMLI for generating a higher number of voltage levels with reduced number of components is achieved on the basis of structural modification. The mathematical analysis for determination of capacitance, power loss analysis and comparative analysis has been provided in detail. A comprehensive comparison with other similar topologies is also provided to highlight the merits of the proposed topology. Simulation and experimental results are discussed for various dynamic load conditions with different output frequencies to validate the suitability of the proposed SCMLI for various high-frequency AC applications, such as renewable energy systems, microgrids, electric vehicles and so on.

1 Introduction

NASA has introduced the high-frequency AC (HFAC) power distribution system (PDS) for space applications, as it offers several merits over the conventional DC power distribution [1, 2]. HFAC PDS is also an attractive solution to other applications like telecom, electric vehicles and renewable energy microgrids. The high-frequency inverters have advantages like reduced high-order harmonics and low current ripple harmonics in induction motor drives [3]. Power converters play a major role in microgrids due to their advantages like being efficient, reliable, managed heat distribution and high power density [3]. Multilevel inverters (MLIs) are one of the emerging converters owing to their several structural benefits in terms of easy extension, reduced voltage stress (dv/dt) and having equal load sharing and efficient energy harvesting making them highly suitable for various renewable energy applications [4]. Among several MLIs, switched capacitor MLIs (SCMLIs) are the most widely used because of the features of voltage boosting over conventional ones with reduced number of DC sources [5]. To generate a higher number of voltage levels, cascaded MLIs are taken into consideration aiming for reduced number of devices but it ends up having high blocking voltage and does not ensure the voltage boosting feature [6].

Hybrid MLIs having reduced semiconductor devices ensures their ability to have an increased number of levels either by cascading multiple units into each other or by providing a backend H-bridge, but they suffer from the problems of high blocking voltage with an increased number of semiconductor elements [7–9]. Cascading subunits of the SCMLI to obtain a desired output voltage with an increased number of capacitors attaining parallel connection attains high boosting ratio but suffers high blocking voltage, results in increased switching losses and conduction losses [10, 11]. However, the increased number of DC sources with asymmetric configuration is capable of generating a desired output voltage level [12], but at the price of no boosting ability [13]. A quasi-Z-MLI with multiple switched capacitors are connected in series/parallel to generate high number of voltage level. Even though, the topology uses single DC source, the choosing of resonance circuit (both capacitance and inductance) value is difficult [14]. A boost type inverter with increased number of switches and capacitors to generate a desired output voltage, which results in high cost of implementation as compared to others, is presented in [15]. Several SC cells are being cascaded containing the same number of units in each cell having higher gain ratio with increased power losses, which results in lower efficiency and high heat dissipation because of high blocking voltage [16]. In [17], a topology to generate a step up in voltage by providing isolation on both input and output side switching losses and high dv/dt is presented. Increasing number of power switches with an aim of generating desired output voltage [18]. Cross-switched MLI having high blocking voltage with reduced number of components with multiple structural configuration is proposed in [19]. Employing a single DC source, topology in [20] is very elegant for HFAC power source, however, at the price of increased number of semiconductor devices. An interesting way of cascading H-bridge to acquire higher number of levels in [21] requires high cost of implementation with increased number of sources and capacitor count. Multiple DC sources connected in parallel to each other with series conversion for voltage step up results in high blocking voltage and low efficiency [22]. Despite several attempts to reduce the complexity of the SCMLIs for HFAC PDS, the component count stands still high.

In this paper, a novel five-level (5L) SCMLI is discussed for generating higher number of voltage levels with reduced number of components. The rest of the paper is organised as follows. The basic unit of the proposed 5L converter is discussed in Section 2. Further extended to generation of a nine-level (9L) voltage as discussed in Section 3. Section 4 briefly deals with the extension of proposed 9L-SCMLI on the basis of possible structural modification. Section 5 discusses the design guidelines of the

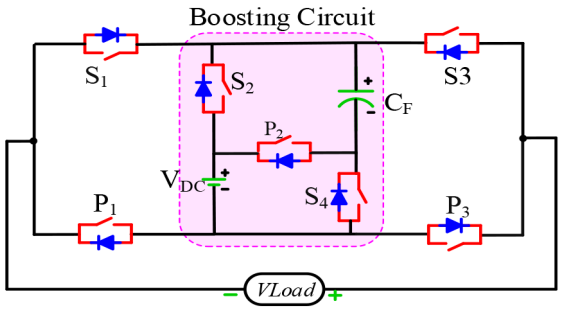


Fig. 1 *Proposed 5L-SCMLI*

Table 1 Switching scheme of 5L-SCMLI

Voltage levels	Switches							Capacitor
	S_1	S_2	S_3	S_4	P_1	P_2	P_3	C_F
$+1V_{dc}$	0	1	1	1	1	0	0	C
$+2V_{dc}$	0	0	1	0	1	1	0	D
0	1	1	1	1	0	0	0	C
$-1V_{dc}$	1	1	0	1	0	0	1	—
$-2V_{dc}$	1	0	0	0	0	1	1	D

required capacitance for the proposed 9L-SCMLI. Further, the detailed equivalent circuit of each mode and power losses analysis is carried out in Section 6. Section 7 details a comparative study of the proposed SCMLIs with other topologies on basis of figure of merits. Section 8 validates the proposed topology and its variants through simulation and experimental tests for high frequency with dynamic load variation at different parameters. Finally, Section 9 concludes the proposed SCMLIs.

2 Basic unit of the proposed 5L-SCMLI

2.1 Circuit topology

Fig. 1 shows the basic unit of the proposed hybrid 5L-SCMLI circuit, from [23]. It consists of a single DC power supply V_{dc}, capacitor C_F, and six switches S_1 to S_4, P_1 to P_3 to generate a peak output voltage of magnitude twice the input voltage. In ideal circumstances, the proposed inverter has five distinct output voltage levels: $\pm 2V_{dc}$, $\pm_{dc}1$ V and 0.

2.2 Description of each voltage level

For the proposed 5L inverter, switching scheme listed in Table 1 includes the state of the diode and capacitor to have a better and quick understanding of the current path for each cycle. At level $+1V_{dc}$, capacitor (C_F) gets charged. Similarly, at level 0 also the capacitor gets charged. While, at level $\pm 2V_{dc}$, capacitor is discharging and its voltage remains unchanged for level $-1V_{dc}$. Therefore, the proposed 5L inverter is equipped with self-voltage balancing and voltage boosting ability with reduced semiconductor elements, decreasing the cost of implementation and as such does not require additional circuit for balancing capacitor voltage, which reduces the complexity in the converter design.

3 Derivation of a new 9L-SCMLI from the proposed 5l-SCMLI BU

3.1 Circuit description

The proposed hybrid 9L-SCMLI topology as shown in Fig. 2 is achieved from the previously introduced basic unit by adding an H-bridge in the backend to change the polarity and capacitors are attached in series/parallel to each other to achieve desired output voltage. The proposed 9L-SCMLI also uses a single DC voltage source (V_{dc}), two capacitors (C_1 and C_2), two diodes (D_1, D_2) and only eight power switches (S_1–S_8) for generating a peak output of

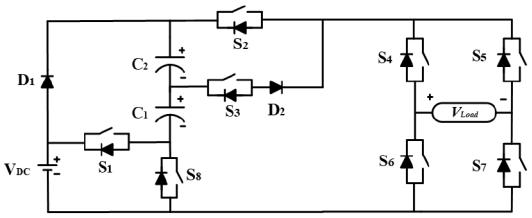


Fig. 2 *Proposed 9L-SCMLI*

twice the input voltage which comprises of nine distinct output voltage levels: $\pm 2V_{dc}$, $\pm 3V_{dc}/2$, $\pm V_{dc}$, $\pm V_{dc}/2$ and 0.

3.2 Modes of operation of the proposed 9L-SCMLI

The different modes of operation and, for a better understanding, current path is also demonstrated in Figs. 3*a–d* for positive half-cycle. Where, i_o represents the direction of current. During $+V_{DC}/2$ and $+V_{DC}$ both capacitors are charged initially generating an output voltage equivalent to $+V_{DC}/2$ and $+V_{DC}$. While, during $+3V_{DC}/2$ capacitor C_1 is discharged to generate output voltage equivalent to $+3V_{DC}/2$. While, during $+2V_{DC}$ both capacitors C_1 and C_2 are discharged collectively generating output voltage equivalent to $+2V_{DC}$ and so on, as during $+V_{DC}$ and $+2V_{DC}$ both capacitors are charged and discharged collectively sharing the same charging and discharging current. Therefore, maintaining the constant output current. Whereas, the primary function of the backend H-bridge is to operate at fundamental cycle and change the polarity of the output voltage switching S_4 and S_7 on for positive half, S_5 and S_6 on for negative half and also to generate zero level as switches S_4 and S_5 are turned on. Some of the prominent features of the proposed 9L-SCMLI has the following features:

(a) Generates output voltage of magnitude twice the input voltage ($V_{out} = 2V_{in}$).
(b) Only eight power switches, two diodes, single source and two capacitors are used to generate desired output voltage requiring reduced number of components are required.
(c) Does not require additional circuits for balancing capacitors voltage as it has self-balancing and self-voltage boosting ability with reduced complexity.

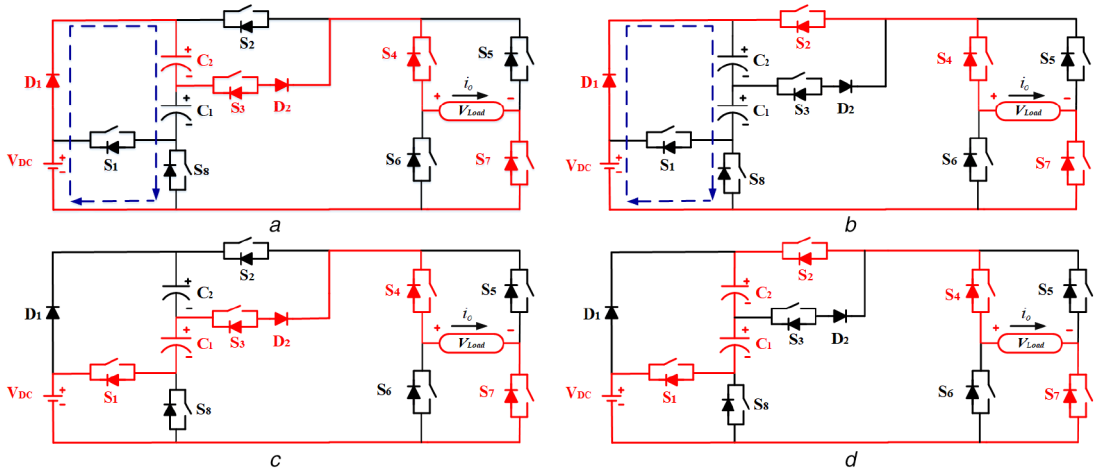


Fig. 3 *Modes of Operation for positive half cycle*
(a) $+V_{DC}/2$ (first positive level), ***(b)*** $+V_{DC}$ (second positive level), ***(c)*** $+3V_{DC}/2$ (third positive level), ***(d)*** $+2V_{DC}$ (fourth positive level)

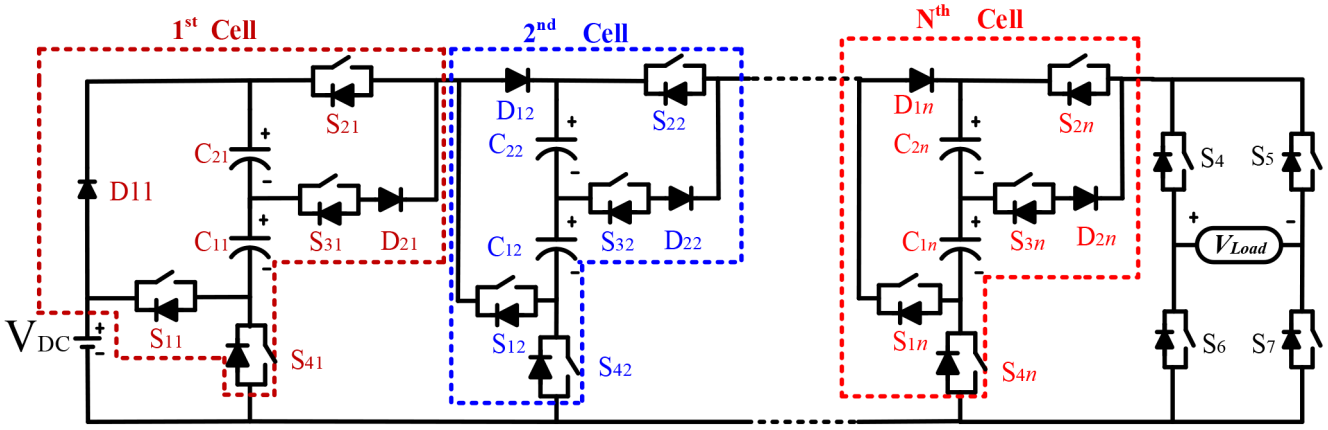


Fig. 4 *HE of the proposed 9L-SCMLI*

4 Extension of the proposed 9L-SCMLI

4.1 Extension occurrence

Proposed 9L-SCMLI can be further extended based on the structural point of view to generate higher number of levels in all possible directions to generate desired output voltage. The possible ways of extension can be achieved in two ways: horizontal extension (HE) and vertical extension (VE), which are discussed in detail below.

4.2 Horizontal extension

Fig. 4 shows the extension of the proposed 9L-SCMLI in horizontal direction to generate higher number of levels and is here after referred to as 9L-SCMLI (HE). It can be extended up to *N*th cell as 1st cell, 2nd cell … *N*th cell. Each cell contains a desired number of units having same configuration throughout the circuit up to its extension, which can be extended as (S_{11}, S_{12}, S_{13}…, S_{1n}). Similarly, (S_{21}, S_{22}, S_{23}, …, S_{2n}), (S_{31}, S_{32}, S_{33}, …, S_{3n}) and (S_{41}, S_{42}, S_{43}, …, S_{4n}); while diodes (D_{11} and D_{21}) and capacitors (C_{11} and C_{21}) are extended in the same manner. As capacitors (C_{11} and C_{21}) are connected parallel to each other, it provides a step up in voltage. Further, operation of the proposed 9L-SCMLI (HE) is discussed in brief.

Generalised switching pattern of the proposed 9L-SCMLI (HE) is listed in Table 2, which can be generated with the help of Fig. 4 as it represents the extension of the proposed 9L-SCMLI in horizontal direction up to *n*. Further, the charging and discharging of capacitors (C_{11}, C_{12}, C_{13}, …, C_{1n}) and (C_{21}, C_{22}, C_{23}, …, C_{2n}) are similar to Table 2. When opted for higher number of voltage levels, capacitors are charged for a longer period. While, discharging period of capacitors decreases for higher number of voltage levels. In order to validate the following results, generalised equations (1)–(6) are provided.

$$N_L = 4n + 1 \tag{1}$$

$$N_{\text{cap}} = 2(n-1) \tag{2}$$

$$N_d = 2(n-1) \tag{3}$$

$$N_{\text{sw}} = N_{\text{driver}} = 4n \tag{4}$$

$$V_{\max} = nV_{\text{dc}} \tag{5}$$

$$V_{\text{in}} : V_{\text{out}} = 1 : n \tag{6}$$

where N_{sw} represents number of switches, N_{cap} is the number of capacitors, N_D is the number of diodes, N_L is the number of voltage levels and $V_{\max}$ is the maximum output voltage, where, n is dependent upon maximum gain to be generated as it satisfies the condition $n \geq 2$.

4.3 Vertical extension

Fig. 5 shows the extension of the proposed 9L-SCMLI in a vertical configuration and hereafter referred to as 9L-SCMLI (VE). As it can be extended up to *N*th cell, each cell containing an acquired number of units of two switches (S_{12},S_{22}…,S_{n2}) and (S_{14}, S_{24}, …, S_{n4}), three diodes (D_{11}, D_{21}, …, D_{n1}) and (D_{12}, D_{22}, …, D_{n2}) and two capacitors (C_{11}, C_{12}, …, C_{1n}) and (C_{12}, C_{22}, …, C_{n2}) connected in parallel to each other to provide a stepped up output voltage. Equations (7)–(12) correspond to 9L-SCMLI (VE) for extending up to n and can be validated with the help of Fig. 5.

Where, n is dependent upon maximum gain to be generated as it satisfies the condition $n \geq 2$. Generalised switching pattern of the proposed extension can be seen from Table 3 for generating $(n+1)$ V_{dc} voltage levels. Further, comparison of the proposed 13L-SCMLI (VE) with other topologies is carried out in Section 7. Charging and discharging of capacitors with respect to desired voltage level can be seen from Table 3

$$N_L = 4n + 1 \tag{7}$$

$$N_{cap} = 2(n-1) \tag{8}$$

$$N_d = 2(n-1) \tag{9}$$

$$N_{sw} = N_{driver} = 3n + 2 \tag{10}$$

$$V_{max} = nV_{dc} \tag{11}$$

$$V_{in} : V_{out} = 1 : n \tag{12}$$

5 Determination of capacitance

The determination of a suitable capacitance value is another important factor for SCMLI topologies. Here, the determination of capacitance for the proposed 9L-SCMLI is discussed. For determining the value of capacitance, longest discharging cycle (LDC) of each capacitor is taken into account. To aid this, Fig. 6 representing the waveform of the proposed 9L-SCMLI at fundamental frequency is included.

As evident, LDC for both capacitors C_1 and C_2 occur in both positive and negative cycles at different time intervals from

Table 2 Generalised switching pattern for the proposed HE

Output voltage (V_o)	On state of switches					Diodes conducting state		Capacitor states	
	$S_{11},S_{12},\ldots,S_{1n}$	$S_{21},S_{22},\ldots,S_{2n}$	S_{31},S_{32},S_{3n}	$S_{41},\ldots,S_{4n}$	S_4,S_5,S_6,S_7	$D_{11},\ldots,D_{1n}$	$D_{21},\ldots,D_{2n}$	$C_{11},\ldots,C_{1n}$	$C_{21},\ldots,C_{2n}$
$+V_{dc}/2$	-,…,-	$S_{21}\ldots S_{2(n-1)}$	S_{3n},-…-	$S_{41}\ldots S_{4n}$	S_4,S_7	$D_{11}\ldots D_{1n}$	-…-, D_{2n}	$C,C\ldots,C$	$C,C\ldots,C$
$+V_{dc}$	-,…,-	$S_{21}\ldots S_{2n}$	-…-	$S_{41}\ldots S_{4n}$	S_4,S_7	$D_{11}\ldots D_{1n}$	-,…,-	$C,C\ldots,C$	$C,C\ldots,C$
$+3V_{dc}/2$	-…-,S_{1n}	$S_{21}\ldots S_{2(n-1)}$	S_{3n},-…-	$S_{41}\ldots S_{4(n-1)}$	S_4,S_7	$D_{11}\ldots D_{1(n-1)}$	-…- ,D_{2n}	$C,\ldots,C, D$	$C,\ldots C,$-
$+2V_{dc}$	-…-,S_{1n}	$S_{21}\ldots S_{2(n-1)}$	-,…-	$S_{41}\ldots S_{4(n-1)}$	S_4,S_7	$D_{11}\ldots D_{1(n-1)}$	-,…,-	$C,\ldots,C, D$	$C\ldots C, D$
$+5V_{dc}/2$	-…-$S_{1(n-1)}$ S_{1n}	$S_{21}\ldots S_{2(n-2)}$	$S_{3(n-1)}$,-…-	$S_{41}\ldots S_{4(n-2)}$	S_4,S_7	$D_{11}\ldots D_{1(n-2)}$	-…-,$D_{2(n-1)}$	$C\ldots C,D, D$	$C\ldots C,$-, D
$+3V_{dc}$	-…-$S_{1(n-1)}$ S_{1n}	$S_{21}\ldots S_{2(n-2)}$	-,…-	$S_{41}\ldots S_{4(n-2)}$	S_4,S_7	$D_{11}\ldots D_{1(n-2)}$	-,…,-	$C\ldots C,D$ D	$C\ldots C,D$ D
…	…	…	…	…	…	…	…	…	…
$+(n+1)V_{dc}$	$S_{11}\ldots S_{1n}$	$S_{21}\ldots S_{2n}$	-,…,-	-,…,-	S_4,S_7	-,…,-	-,…,-	$D,D,\ldots,D$	$D,D,\ldots,D$
$-(n+1)V_{dc}$	$S_{11}\ldots S_{1n}$	$S_{21}\ldots S_{2n}$	-,…,-	-, …,-	S_5,S_6	-,…,-	-,…,-	$D,D,\ldots,D$	$D,D,\ldots,D$
$0.V_{dc}$	-,…,-	-,…,-	-,…-	-,…,-	S_4,S_5	-,…,-	-,…,-	-,…,-	-,…,-

-, OFF state; …, continuation of previous states.

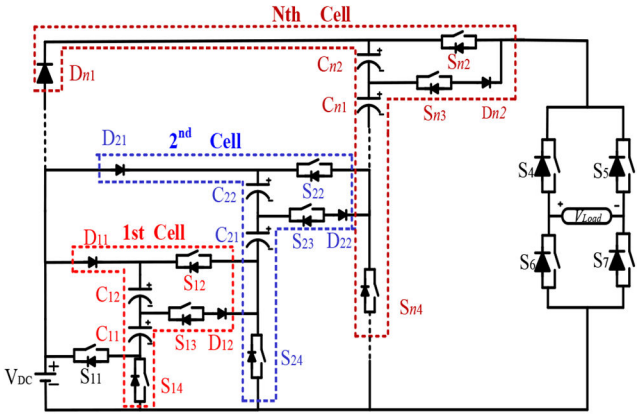


Fig. 5 *VE of the proposed 9L-SCMLI*

Table 3 Generalised switching pattern for the proposed VE

Output voltage (V_o)	On state of switches					Diodes conducting state		Capacitor states	
	S_{11}	$S_{n2.\|.}S_{22},$ S_{12}	$S_{n3}\ldots S_{23}S_{13}$	$S_{n4}\ldots S_{24}S_{14}$	S_4,S_5,S_6,S_7	$D_{n1}\ldots D_{21},D_{11}$	$D_{n2}\ldots D_{22},D_{12}$	$C_{n1}\ldots$ C_{21},C_{11}	$C_{n2}\ldots$ C_{22},C_{12}
$+V_{dc}/2$	-,…,-	-,…-	S_{n3},-…,-	$S_{n4}\ldots S_{24},S_{14}$	S_4,S_7	$D_{11},D_{21}\ldots D_{n1}$	D_{n2},-,…,-	$C,C,\ldots,C$	$C,C,\ldots,C$
$+V_{dc}$	-,…,-	S_{n2},-,…,-	-,…,-	$S_{n4}\ldots S_{24},S_{14}$	S_4,S_7	$D_{11},D_{21}\ldots D_{n1}$	-,…,-	$C,C,\ldots,C$	$C,C,\ldots,C$
$+3V_{dc}/2$	-,…,-	$S_{(n-1)2}$,-…-	S_{n3},-…-	$S_{(n-1)4},\ldots,S_{14}$	S_4,S_7	$D_{(n-1)1},\ldots,D_{11}$	D_{n2},-,…,-	$D,C,\ldots,C$	-,$C,C,\ldots,C$
$+2V_{dc}$	-,…,-	$S_{n2},S_{(n-1)2}$-…	-,…,-	$S_{(n-1)4},\ldots,S_{14}$	S_4,S_7	$D_{(n-1)1},\ldots,D_{11}$	-,…,-	$D,C,\ldots,C$	$D,C,\ldots,C$
$+5V_{dc}/2$	S_{11}	-,…,-	$S_{(n-1)3}$,-…-	$S_{(n-2)4},\ldots,S_{14}$	S_4,S_7	$D_{(n-2)1},\ldots,D_{11}$	$D_{(n-1)2},\ldots,D_{12}$	$D,D,C,\ldots,C$	D,-,$C,\ldots,C$
$+3V_{dc}$	S_{11}	S_{n2},-,$S_{(n-2)}$-.	-,…-	$S_{(n-2)4},\ldots,S_{14}$	S_4,S_7	$D_{(n-2)1},\ldots,D_{11}$	-,…,-	$D,D,C,\ldots,C$	$D,D,C,\ldots,C$
…	…	…	…	…	…	…	…	…	…
$+(n+1)V_{dc}$	-,S_{11}…	$S_{n2},\ldots,S_{12}$	-,…,-	$S_{(n-1)4},\ldots,S_{14}$	S_4,S_7	$D_{(n-1)1},\ldots,D_{11}$	-,…,-	$D,D,\ldots,D$	$D,D,\ldots,D$
$-(n+1)$ V_{dc}	-,S_{11}…	$S_{n2},\ldots,S_{12}$	-,…,-	$S_{(n-1)4},\ldots,S_{14}$	S_5,S_6	$D_{(n-1)1},\ldots,D_{11}$	-,…,-	$D,D,\ldots,D$	$D,D,\ldots,D$
$0.V_{dc}$	-,…-	-,…,-	-,…,-	-,…,-	S_4,S_5	-,…,-	-,…,-	-,…,-	-,…,-

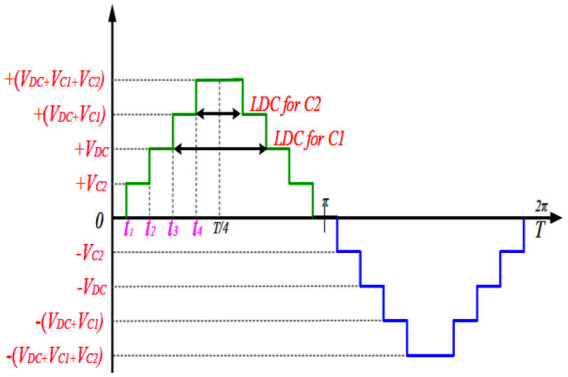


Fig. 6 *Nine-level output voltage waveform*

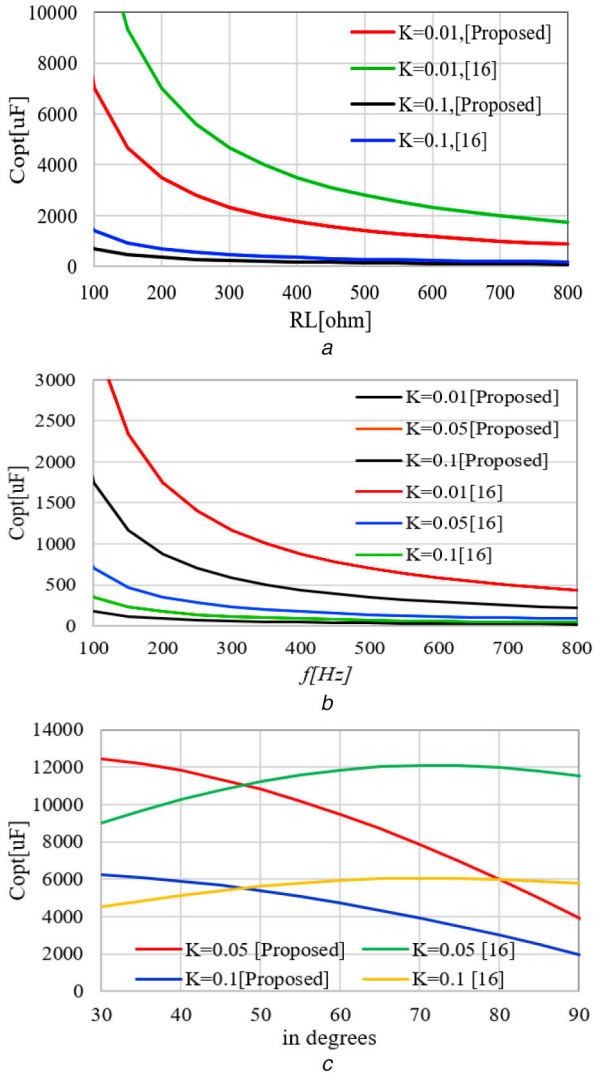


Fig. 7 *Variation of optimal capacitance (Copt) versus*
(a) RL (resistive load), ***(b)*** *f* (frequency), ***(c)*** Phase angle (Φ)

different voltage levels. Therefore, maximum discharging value for each capacitor can be concluded from the following equations:

$$Q_C1 = 2 \times \int_{t_3}^{T/4} I_L(t)\,\mathrm{d}t\,. \tag{13}$$

$$Q_{C2} = 2 \times \int_{t_4}^{T/4} I_L(t)\,\mathrm{d}t\,. \tag{14}$$

Here, Q_{Ci} for = 1, 2 represents the maximum discharging amount of capacitors. In equation, $k \times V_{\mathrm{dc}}$ represents maximum allowable voltage ripple of capacitors, optimum value of capacitors can be obtained from

$$C_{\mathrm{opt}}, i \geq \frac{Q_{Ci}}{k \times V_{\mathrm{dc}}} \tag{15}$$

Considering the equation of load current for a pure resistive load (R_L) at third and fourth positive output voltages at steady-state conditions, the following can be derived:

$$I_L(t) = \frac{3V_{\mathrm{dc}}}{2R_L}, \quad t_3 \leq t \leq \frac{T}{4} \tag{16}$$

$$I_L(t) = \frac{2V_{\mathrm{dc}}}{R_L}, \quad t_4 \leq t \leq \frac{T}{4} \tag{17}$$

Further the fundamental switching timing instants t_3 and t_4 are equal to $3T/20$ and $T/5$ and are obtained from cutting of DC levels to sinusoidal function of reference waveform. For resistive-inductive loading condition function $I_{\mathrm{L}}(t)$ can be expressed as

$$I_L(t) = I_{\mathrm{max}}\sin(\omega t - \phi) \tag{18}$$

By solving (13)–(18) at given conditions, the optimum value of capacitors at pure resistive load and resistive-inductive load are shown in the following equation:

$$\mathrm{Copt}, i \geq \frac{7\pi}{10R_L \times k \times \omega} \tag{19}$$

$$\mathrm{Copt}, i \geq \frac{2I_{\mathrm{max}}}{k \times V_{\mathrm{dc}} \times \omega}\left[\cos\left(\frac{\pi}{10} - \phi\right) + \sin\left(\frac{2\pi}{5} + \phi\right)\right] \tag{20}$$

It is worth mentioning that (19) and (20) represent the optimum value of capacitors for the proposed 9L-SCMLI, which shows an inverse relation with k, ω and R_L from (19). To have a better understanding for determining appropriate value of capacitance, a graph is shown in Fig. 7*a* between C_{opt} and R_L at different values for an allowable voltage ripple keeping ω fixed at the value 100π. From Fig. 6*b*, it can be concluded that a larger rate of allowable voltage ripple has led to smaller capacitance. By increasing the output frequency at different values of R_L, the value of optimum capacitance gets reduced but may lead to increase in switching losses at higher output frequency. In order to provide a better clarification, a graph is being plotted between different variations of C_{opt} at different values of output frequency at fixed resistive load $R_L = 200\ \Omega$ for higher frequency at allowable voltage ripple.

On the other hand, optimum capacitance is varied for different angles of ϕ at allowable voltage ripple of 5 and 10%, where $k =$ 0.05 and $k = 0.1$, considering a constant value for $I_{\mathrm{max}} = 5$ A, V_{DC} = 100 V, $f = 50$ Hz and $\omega = 100\pi$ at fundamental frequency. It can be concluded that as ϕ increases the value of capacitance decreases for the proposed SCMLI as shown in Fig. 7*c*.

6 Power loss analysis

In this section, power loss analysis of the proposed 9L-SCMLI is being considered [16]. It includes overall loss calculation; switching losses P_{Sw}, conduction losses P_{Con} and ripple losses P_{Rip} for both capacitors at fundamental frequency as maximum loss conditions are considered during calculations.

6.1 Switching losses

In general, switching losses occur during ON and OFF transition state of switches. To reduce the complexity, a linear approximation between voltage and current of switches is being considered for switching period. As an outcome, following equations are considered for switching losses:

$$P_{\text{sw,on},i} = \int_0^{t_{\text{on}}} v(t)i(t)\,\mathrm{d}t = \int_0^{t_{\text{on}}} \left[\left(\frac{V_{\text{sw},i}}{t_{\text{on}}}t\right)\left(-\frac{I_i}{t_{\text{on}}}(t-t_{\text{on}})\right)\right]\cdot \mathrm{d}t = \frac{1}{6}V_{\text{sw},i}I_i t_{\text{on}} \quad (21)$$

$$P_{\text{sw,off},i} = \int_0^{t_{\text{off}}} v(t)i(t)\cdot \mathrm{d}t = \int_0^{t_{\text{off}}} \left[\left(\frac{V_{sw,i}}{t_{\text{off}}}t\right)\left(-\frac{I'_i}{t_{\text{off}}}(t-t_{\text{off}})\right)\right]\cdot \mathrm{d}t = \frac{1}{6}V_{\text{sw},i}I'_i t_{\text{off}} \quad (22)$$

where I_i and I'_i are currents through ith switch, N_{on} and N_{off} is number of turn on and off a switch during fundamental cycle k. As a result to calculate total switching loss per one cycle can be written as follows:

$$P_{\text{sw},i} = \frac{1}{6T}\sum_{i=1}^{7}\left(\sum_{k=1}^{N_{\text{on}}} P_{\text{sw,on},ik} + \sum_{k=1}^{N\text{off}} P_{\text{sw,off},ik}\right) \quad (23)$$

6.2 Conduction losses

In order to calculate total conduction losses at steady state, a pure resistive load (R_L) is considered. Based on the overall circuit analysis shown in Figs. 8*a–d*, all possible operations are considered to calculate the maximum conduction loss. Figs. 8*a–d* represent the equivalent circuit diagram for the proposed 9L-SCMLI. Pure resistive loading condition is considered because there should not exist any auxiliary current path between load current and output voltage to facilitate the charging of capacitors. Therefore, resistive loading condition is considered as worst condition for calculation of losses in SCMLIs.

Hereafter, R_{onD}, R_{ESR}, R_{onu} represent internal resistance of power diode, equivalent series resistance of each capacitor and internal resistance of each switch. While V_{RS}, V_{C} and V_{F} showcases reverse biased voltage of power diode, stored voltage of capacitor and forward biased voltage of power diode. By applying Kirchhoff's voltage law and Kirchhoff's current law for connecting nodes, following equations are summarised. Equation (24) represents the charging current of involved capacitors for states $\pm V_{\text{dc}}/2$ during operating mode ($I_{L,\,I}$). Similarly, in (25) for V_{dc} as it also involves charging of capacitors at second operating mode ($I_{L,\,\text{II}}$). Equations (27) and (28) show third and fourth operating modes with respect to Figs. 7*c* and *d*, respectively. Instantaneous value of conduction losses during operating modes I, II, III and IV are given in (28)–(31) as follows:

$$2(R_{\text{onD}}+R_{\text{ESR}})I_{\text{charging}} + (3R_{\text{onu}}+R_{\text{onD}}+R_L)I_{L,I} + R_{\text{onD}}(I_{\text{charging}}+I_{L,I}) = V_{\text{dc}} - V_{\text{RS}} - 2(V_{\text{c}}+V_{\text{F}}) \quad (24)$$

$$2(R_{\text{onD}}+R_{\text{ESR}})I_{\text{charging}} + (3R_{\text{onu}}+R_L)I_{L,\text{II}} + (I_{L,\text{II}}+I_{\text{charging}})R_{\text{onD}} = V_{\text{dc}} - V_{\text{F}} - 2V_{\text{c}} - V_{\text{RS}} \quad (25)$$

$$(4R_{\text{onu}}+R_{\text{onD}}+R_L+R_{\text{ESR}})I_{L,\text{III}} = V_{\text{dc}} - V_{\text{F}} + V_{\text{c}} \quad (26)$$

$$(4R_{\text{onu}}+R_{\text{L}}+2_{\text{ESR}})I_{L,\text{IV}} = V_{\text{dc}} + 2V_{\text{c}} \quad (27)$$

As an outcome, to calculate the average value during full cycle of output voltage waveform for first, second, third and fourth voltage levels, corresponding time should be taken into consideration

$$P_{\text{con}\cdot\text{I}} = 2(I_{\text{charging}})^2(R_{\text{onD}}+R_{\text{ESR}}) + (I_{L,\text{I}})^2(3R_{\text{onu}}+R_{onD}) + R_{\text{onD}}(I_{L,\text{I}}+I_{\text{charging}})^2 \quad (28)$$

$$P_{\text{con,II}} = 2(R_{\text{onD}}+2R_{\text{ESR}})(I_{\text{charging}})^2 + 3R_{\text{onu}}(I_{L.\text{II}})^2 + R_{\text{onD}}(I_{L,\text{II}}+I_{\text{charging}})^2 \quad (29)$$

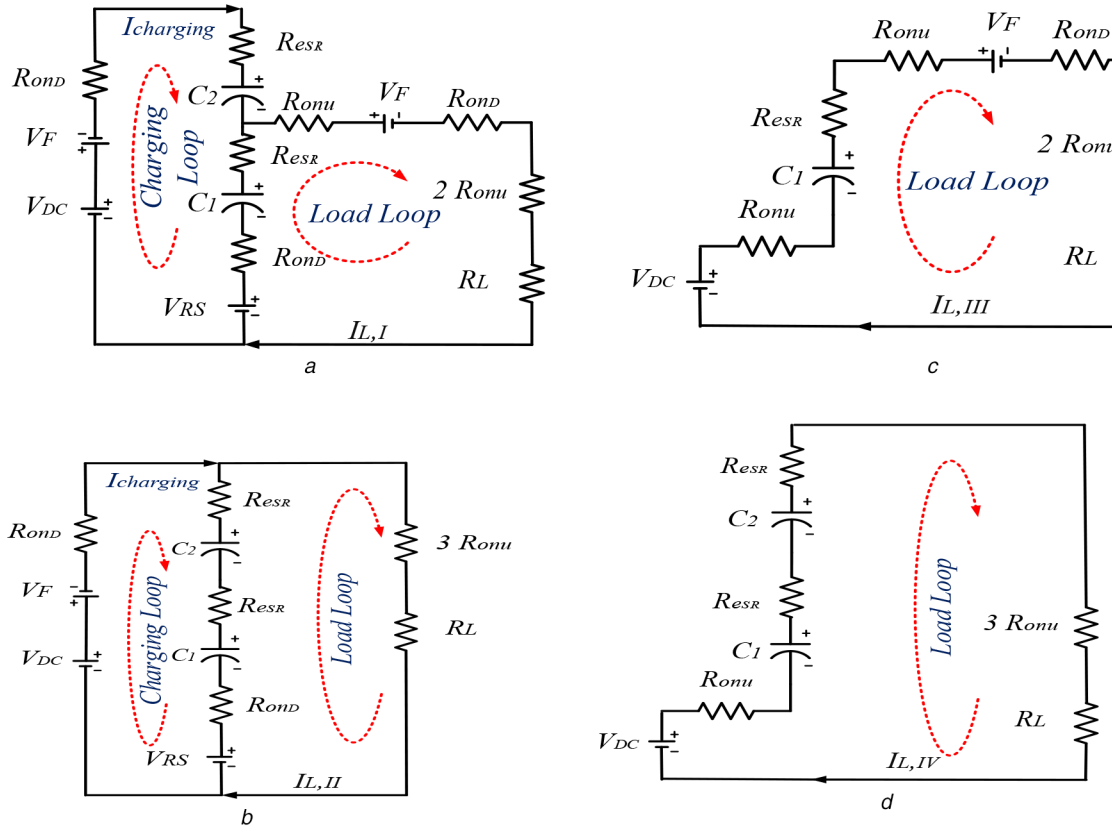


Fig. 8 *Equivalent circuit diagram of the proposed 9L-SCMLI at different modes for (level I–level IV)*
(a) $\pm V_{\text{dc}}/2$, ***(b)*** $\pm V_{\text{dc}}$, ***(c)*** $\pm 3V_{\text{dc}}/2$, ***(d)*** $\pm 2V_{\text{dc}}$

$$P_{\text{con,III}} = (4R_{\text{onu}} + R_{\text{onD}} + R_{\text{ESR}})(I_{L,\text{III}})^2 \quad (30)$$

$$P_{\text{con,IV}} = (4R_{\text{onu}} + 2R_{\text{ESR}})(I_{L,\text{IV}})^2 \quad (31)$$

From Figs. 8*a–d*, $(t_2 - t_1)$, $(t_3 - t_2)$, $(t_4 - t_3)$ and $(T/4 - t_4)$, respectively, are given in (32)–(35). As a result, the total conduction losses ($P_{\text{con,T}}$) over a full cycle output voltage are shown in (36)

$$\overline{P}_{\text{con,I}} = \frac{4}{T}(t_2 - t_1)P_{\text{con,I}} \quad (32)$$

$$\overline{P}_{\text{con,II}} = \frac{4}{T}(t_3 - t_2)P_{\text{con,II}} \quad (33)$$

$$\overline{P}_{\text{con,III}} = \frac{4}{T}(t_4 - t_3)P_{\text{con,III}} \quad (34)$$

$$\overline{P}_{\text{con,IV}} = \frac{4}{T}\left(\frac{T}{4} - t_4\right)P_{\text{con,IV}} \quad (35)$$

$$P_{\text{con},T} = \overline{P}_{\text{con,I}} + \overline{P}_{\text{con,II}} + \overline{P}_{\text{con,III}} + \overline{P}_{\text{con,IV}} \quad (36)$$

6.3 Power loss results

Simulation results for power losses are compared in this section under dynamic load, where, conduction and switching losses of the proposed 9L-SCMLI are calculated for each switch. Figs. 9*a–d* demonstrate the outcomes from loss calculation as discussed above, where $P_{\text{con\_sw}}$, $P_{\text{sw\_sw}}$ represent conduction and switching losses in IGBT and $P_{\text{con\_d}}$, $P_{\text{sw\_d}}$ represent conduction and switching losses in diode.

Only switch S_8 experiences maximum loss as compared to other switches. While switches present in H-bridge, that is S_4, S_5, S_6 and S_7 share almost equal losses and switch S_3 having the least. Overall, power loss for proposed topology is quite low.

6.4 Ripple losses of capacitors

Ripple losses usually occur when capacitors are connected in parallel for charging operation due to the difference between input voltage and voltage of capacitors. Therefore, voltage ripple of capacitors is shown in the following equation:

$$\Delta V_{Ci} = \frac{1}{C_i}\int_{t'}^{t} i_{C_i}(t) \cdot \mathrm{d}t \quad (37)$$

where $[t - t']$ represents time interval of discharging modes in capacitors. Total value of ripples losses for a fundamental cycle can be seen from

$$P_{\text{Rip}} = \frac{1}{2T}\sum_{i=1}^{2} C_i \Delta V_{Ci}^2 \quad (38)$$

Since P_{Rip} is inversely proportional to the capacitance C_i, larger value of capacitance leads to increase in overall efficiency. Equations (39) and (40) represent total losses using which the overall efficiency of the proposed 9L-SCMLI can be deduced as below, where P_{out} is output power of the proposed SCMLI

$$P_{\text{Loss}} = P_{\text{Rip}} + P_{\text{Con},T} + P_{\text{sw}} \quad (39)$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{Loss}}} \quad (40)$$

7 Comparison of the proposed SCMLIs with other topologies

A wide comparison is carried out with other SCMLIs presented in [6–22] as shown in Table 4 on the basis of number of switches (N_{switches}), drivers (N_{drivers}), diodes (N_{diodes}), capacitors (N_{cap}), output voltage level (N_L), maximum blocking voltage (MBV), total voltage stress per unit (TSV_{pu}) and cost function (CF). TSV_{pu} represents the ratio of sum of individual MBV of switches to the peak output voltage level. CF can be calculated as in (41), where weight coefficient (β) varies from 0.5 to 1.5

$$CF = (N_{\text{Switches}} + N_{\text{drivers}} + N_{\text{Diode}} + N_{\text{cap}}) \times \beta\text{TVS} \quad (41)$$

As compared to other SCMLIs, the proposed SCMLI variants have the lowest CF/N_L and TSV_{pu}, which can be observed from Table 4

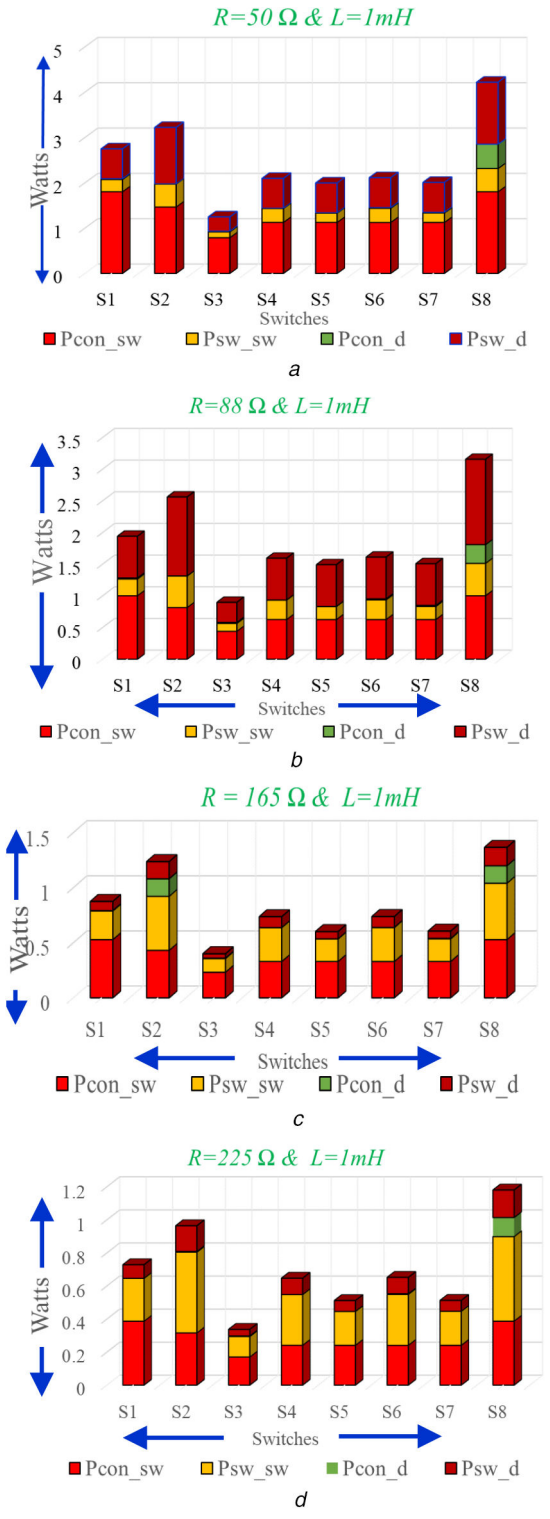


Fig. 9 *Power loss comparison for the proposed 9L-SCMLI at f (fundamental frequency) = 50 Hz*
(a) 50Ω-1 mH, ***(b)*** 88Ω-1 mH, ***(c)*** 165Ω-1 mH, ***(d)*** 225Ω-1 mH

Table 4 Comparison assessment of the proposed SCMLI with other topologies

SCMLI proposed in	N_L	N_{dc}	$N_{drivers}$	$N_{switches}$	N_{diodes}	N_{cap}	MBV	V_{in}:V_{out}	CF/N_L		TVS_{pu}	Voltage boosting
									$\beta = 0.5$	$\beta = 1.5$		
[6]	9	2	12	12	—	4	$4V_{in}$	1:1	56	110.5	8	no
	13	3	16	16	—	6	$6V_{in}$	1:1	83	164.5	9	no
[7]	9	1	10	10	3	3	$4V_{in}$	1:4	42.25	83	5.5	yes
	13	1	14	14	5	5	$6V_{in}$	1:6	71.25	141	6.5	yes
[8]	9	2	12	12	2	2	$2V_{in}$	1:2	77	152.5	10	yes
	13	3	18	18	3	3	$2V_{in}$	1:2	63	124.5	5	yes
[9]	9	1	8	8	6	3	$4V_{in}$	1:4	47.5	93.5	6	yes
	13	1	10	10	10	5	$6V_{in}$	1:6	97.5	193.5	9	yes
[10]	9	2	10	10	2	2	$4V_{in}$	1:2	36	70.5	5	yes
[11]	9	1	12	12	3	3	$4V_{in}$	1:4	54.375	107.25	6.25	yes
[12]	13	2	14	14	—	2	$5V_{in}$	1:3	45.31	89.12	5.33	yes
[13]	9	4	10	10	—	—	$6V_{in}$	1:1	105	208.5	20	no
[14]	9	1	10	10	4	4	$1V_{in}$	1:1	57.75	114	7.25	no
	13	1	14	14	6	6	$1V_{in}$	1:1	95	188.5	8.5	no
[15]	9	1	12	12	—	3	$4V_{in}$	1:4	49.5	97.5	7	yes
[16]	9	1	10	10	1	2	$4V_{in}$	1:4	39	76.5	6	yes
[17]	9	1	9	9	4	1	$4V_{in}$	1:4	42.375	83.25	5.75	yes
[18]	9	1	11	11	—	2	V_{in}	1:2	36.75	72	5.5	yes
[19]	13	2	16	16	2	4	$6V_{in}$	1:3	20.32	39.14	5.6	yes
[20]	13	2	16	16	4	4	$6V_{in}$	1:3	60.4	119.3	5.33	yes
[21]	9	2	9	9	2	2	$2V_{in}$	1:2	63.3	125.1	6.5	yes
[22]	9	1	14	14	—	3	$4V_{in}$	1:4	41.25	81	7.75	yes
	13	1	20	20	—	5	$6V_{in}$	1:6	62.75	124	8.16	yes
[23]	9	1	12	12	—	2	$2V_{in}$	1:4	94.1	186.7	5.25	yes
proposed SCMLI	9	1	8	8	2	2	$2V_{in}$	1:2	26.8	52.1	4.36	yes
	13(VE)	1	11	11	4	4	$3V_{in}$	1:3	50.16	98.82	4.88	yes
	13(HE)	1	12	12	4	4	$3V_{in}$	1:3	44.1	86.7	5.27	yes

Table 5 Comparison of loss distribution in proposed 9L-SCMLI with other relevant 9L topologies

Devices	Proposed in [8]				Proposed in [21]				Proposed in [22]				Proposed 9L-SCMLI			
	con_sw	sw_sw	con_d	sw_d	con_sw	sw_sw	con_d	sw_d	con_sw	sw_sw	con_d	sw_d	con_sw	sw_sw	con_d	sw_d
S_1	0.77	0.16	0.002	0.0516	0.12	0.24	0.007	0.02	0.698	0.15	0.0042	0.04	1.80	0.27	0.003	0.08
S_2	2.08	0.32	0.001	0.10	1.84	0.42	0.002	0.10	1.65	0.42	0.0045	0.11	1.46	0.50	0.0012	0.15
S_3	1.48	0.092	0.012	0.0312	1.58	0.31	0.04	0.03	1.47	0.12	0.012	0.02	0.78	0.12	0.0034	0.03
S_4	0.48	0.09	0.0015	0.0318	1.22	0.16	0.03	0.01	0.699	0.20	0.017	0.01	1.1251	0.30	0.001	0.09
S_5	0.48	0.06	0.0018	0.0208	1.68	0.45	0.042	0.04	1.78	0.423	0.005	0.041	1.1252	0.20	0.0011	0.06
S_6	1.48	0.064	0.6	0.029	1.42	0.12	0.47	0.043	0.87	0.18	0.009	0.0425	1.124	0.31	0.0036	0.098
S_7	0.49	0.16	0.0019	0.0519	1.87	0.96	0.001	0.041	2.04	0.49	0.001	0.0420	1.1245	0.208	0.0009	0.068
S_8	1.02	0.32	0.003	0.103	1.02	0.51	0.003	0.021	1.47	0.423	0.002	0.072	1.802	0.51	0.535	0.171
S_9	0.48	0.09	0.037	0.0315	1.24	0.124	0.037	0.042	1.27	0.13	0.008	0.053	NA	NA	NA	NA
S_{10}	1.45	0.098	0.029	0.0312	NA	NA	NA	NA	1.12	0.51	0.004	0.042	NA	NA	NA	NA
S_{11}	0.48	0.064	0.038	0.021	NA	NA	NA	NA	1.32	0.121	0.0072	0.047	NA	NA	NA	NA
S_{12}	1.45	0.065	0.018	0.0208	NA	NA	NA	NA	0.87	0.14	0.0042	0.0726	NA	NA	NA	NA
S_{13}	NA	NA	NA	NA	NA	NA	NA	NA	1.86	0.153	0.0076	0.0723	NA	NA	NA	NA
S_{14}	NA	NA	NA	NA	NA	NA	NA	NA	1.78	0.48	0.65	0.15	NA	NA	NA	NA
total loss, W	16.39				19.98				21.10				12.32			
efficiency, %	96.18				95.15				94.06				97.08			

NA , not applicable.

providing in depth comparison depending on various factors required for assessment of the proposed SCMLI with other topologies. The proposed 9L and 13Ls are compared with other recent topologies. In this the improved 9L-inverter uses lower number of power consumption with reduced cost and also the MBV on switch is $3V_{in}$ whereas other topologies blocking voltage is $4V_{in}$. Further, cost of the proposed topology increasing when the current rating of switches are increasing. Compared to HE, the VE uses less number of power components and cost also reduced. Further, loss distribution for 9L-SCMLI is compared with other relevant 9L topologies, under R–L (225 Ω^{-1}mH) load condition at $f = 50$ Hz (fundamental frequency) as shown in Table 5. As

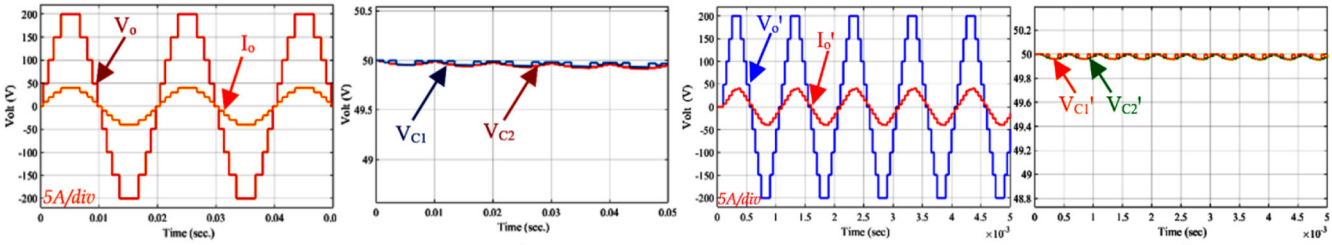


Fig. 10 *Simulation waveforms of the proposed 9L-SCMLI*

(a) Output voltage (V_O) and current (I_O) waveform at $f = 50$ Hz, ***(b)*** Capacitor output voltage waveform (V_{c1} and V_{c2}) at $f = 50$ Hz, ***(c)*** Output voltage (V'_O) and current (I'_o) waveform at $f = 1$ kHz, ***(d)*** Capacitor output voltage waveform (V_{c1} and V_{c2}) at $f = 1$ kHz

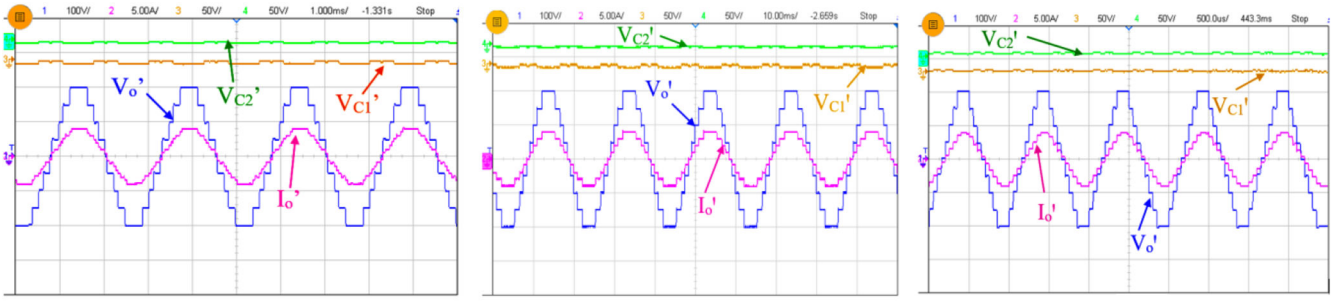


Fig. 11 *Experimental waveforms of the proposed 9L-SCMLI*

(a) Output voltage (V'_O) and current (I'_o) waveform, capacitor output voltage waveform (V'_{c1} and V'_{c2}) at $f = 50$ Hz, ***(b)*** Output voltage (V'_O) and current (I'_o) waveform, capacitor output voltage waveform (V'_{c1} and V'_{c2}) at $f = 400$ Hz, ***(c)*** Output voltage (V'_O) and current (I'_o) waveform, capacitor output voltage waveform (V'_{c1} and V'_{c2}) at $f = 1$ kHz

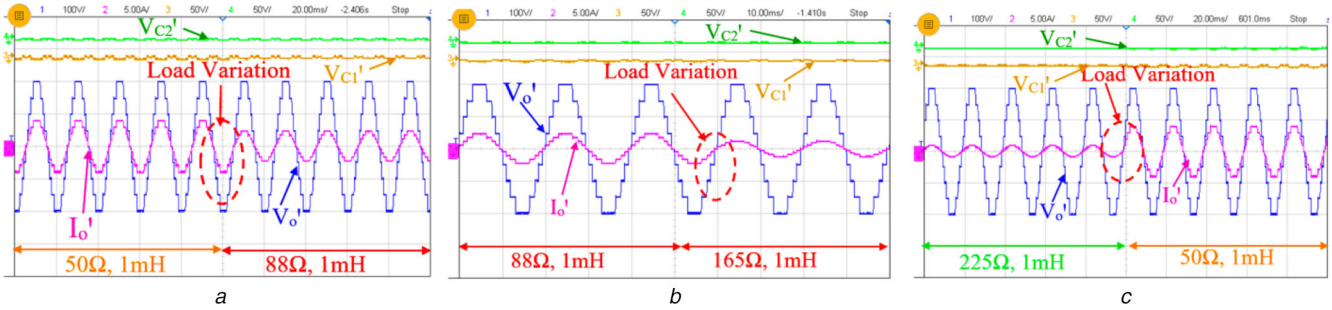


Fig. 12 *Experimental waveforms of the proposed 9L-SCMLI output voltage (V'_O) and current (I'_o) waveform, capacitor output voltage waveform (V'_{c1} and V'_{c2}) having dynamic load variation @ $f = 400$ Hz*

(a) Load variation from 50 Ω, 1 mH to 88 Ω,1 mH, ***(b)*** Load variation from 88 Ω, 1 mH to 165 Ω, 1 mH, ***(c)*** 225 Ω, 1 mH to 50 Ω, 1 mH

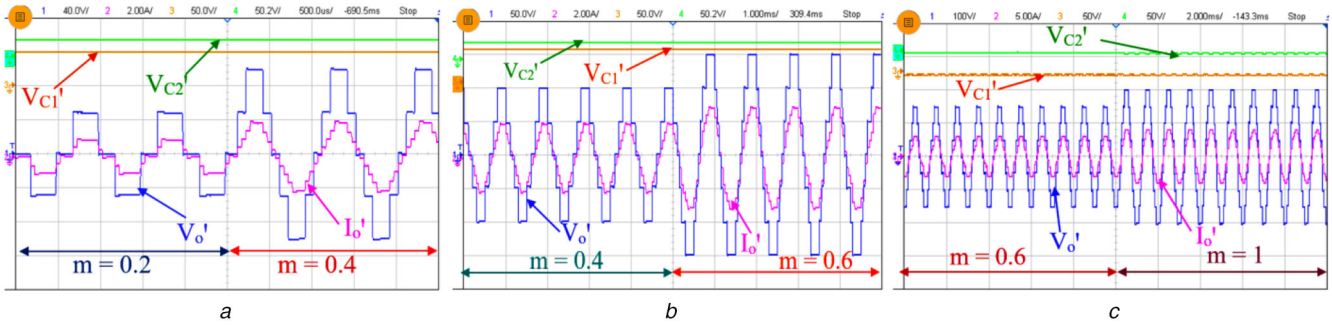
expected, efficiency of the proposed 9L-SCMLI is better with least losses as compared to other proposed topologies.

8 Results and discussion

The simulation and experimental results are discussed in this section to validate the performance of the proposed SCMLI. Firstly, the proposed SCMLIs were simulated in MATLAB/SIMUINK for values $V_{in} = 100$ V with each capacitor of 470 µF having $R_{ESR} = 0.1$ Ω under dynamic load condition for fundamental frequency ($f = 50$ Hz) and $f = 400$ Hz–1 kHz. In order to verify the performance of the proposed SCMLI experimentally, a laboratory prototype was fabricated using Semikron insulated gate bipolar transistors (IGBT SKM75GB063D switches) having $R_{onu} = 14$ mΩ and power diode 25 HMR 120 with $R_{onD} = 3$ mΩ and each capacitor of 470 µF were used. The dSPACE 1104 is used for generating the gate pulses at fundamental frequency of 50 Hz, while SKYPER-32-PRO-R as gate driver were used during implementation of prototype.

8.1 Results of the proposed 9L-SCMLI

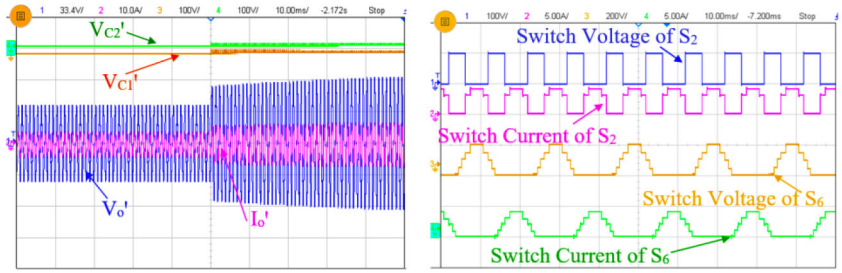
In this section, both simulation waveforms of the proposed 9L-SCMLI at $f = 50$ Hz and 1 kHz are shown in Figs. 10*a–d* under *R–L* ($R = 50$ Ω, $L = 1$ mH) load condition. While, experimental waveforms are shown in Figs. 11*a–c* at $f = 50$ Hz, 400 Hz and 1 kHz under *R–L* ($R = 50$ Ω, $L = 1$ mH) load condition at different frequency having output voltage equal to 200 V and output current equal to 4 A, as both capacitors voltage equal to 50 V. However, waveforms shown in Figs. 11*a–c* represent the performance of the proposed 9L-SCMLI when opted for higher frequency at a fixed load condition. Dynamic load variation is done at $f = 400$ Hz as shown in Figs. 12*a–c*. Waveforms shown in Figs. 11*a–c* highlight the feasibility of the proposed SCMLI for load variation adaptability at higher frequency. Change in modulation index (m) is shown in Figs. 13*a–c*. At m equal to 0.2, 0.4, 0.6 and 1 at f equal to 1 kHz. Fig. 12*a* represents a change in m from 0.2 to 0.4 causing change in output voltage and current waveform while the voltage across both the capacitors remains constant (capacitors are neither charged nor discharged). Similarly, as in Fig. 13*b*, while in Fig. 13*c* voltage across capacitors changes with change in m from 0.6 to 1. In conclusion, during change in m change in output voltage levels is observed as shown in Fig. 13*a* from 3L to 5L, Fig. 13*b* from 5L to 7L, Fig. 13*c* from 7L to 9L. Change in step input voltage from 100 to 200 V is shown in Fig. 14*a*, generally. From low to high causing change in output voltage, current and voltage across capacitors represents the stability of the proposed SCMLI under sudden change in input voltage at $f = 1$ kHz. Switch voltage and current across switches S_2 and S_6 is shown in Fig. 14*b* at $f = 50$ Hz under *R–L* ($R = 50$ Ω, $L = 1$ mH) load condition. Feasibility of the



a *b* *c*

Fig. 13 *Experimental waveforms of proposed 9L-SCMLI output voltage (V'_O) and current (I'_o) waveform, capacitor output voltage waveform (V'_{c1} and V'_{c2}) with change in modulation index (m) at $f = 1$ kHz*

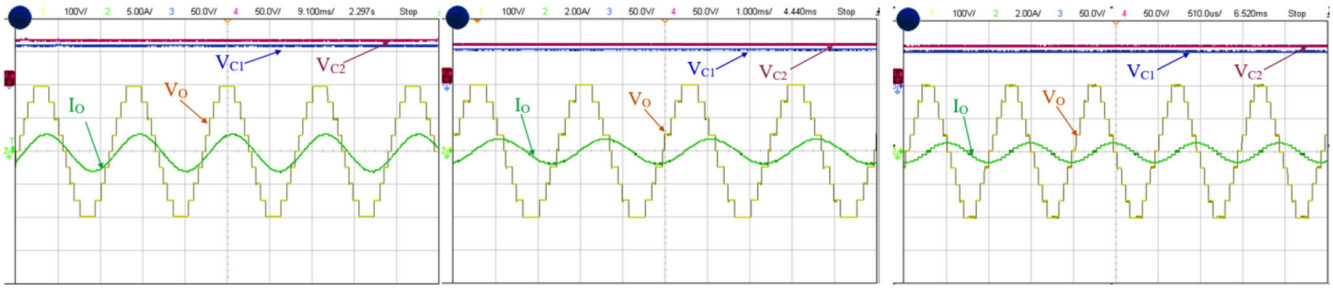
(a) Varying *m* from 0.2 to 0.4, ***(b)*** Varying *m* from 0.4 to 0.6, ***(c)*** Varying *m* from 0.6 to 1



a *b*

Fig. 14 *Experimental waveforms of the proposed 9L-SCMLI output voltage (V'_O) and current (I'_o) waveform, capacitor output voltage waveform (V'_{c1} and V'_{c2})*

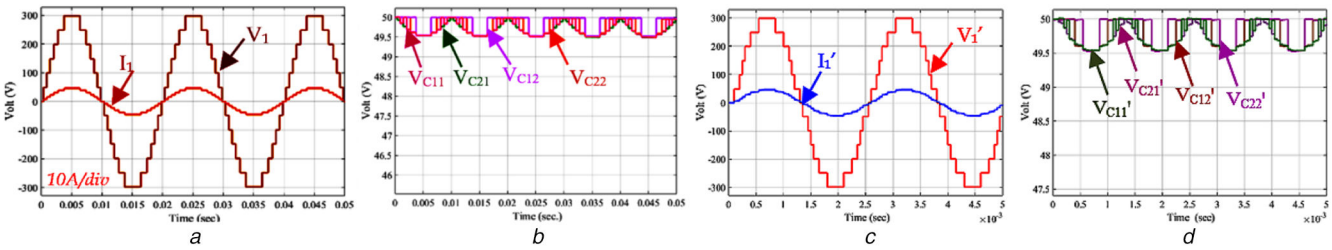
(a) Change in step input voltage (low to high) at $f = 1$ kHz, ***(b)*** Switch voltage and current of S_2 and S_6 at $f = 50$ Hz



a *b* *c*

Fig. 15 *Experimental waveforms of the proposed 9L-SCMLI, output voltage (V_O) and current (I'_o) waveform, capacitor output voltage waveform (V_{c1} and V_{c2}) under R–L (80 Ω–100 mh) load condition*

(a) At $f = 50$ Hz, ***(b)*** At $f = 400$ Hz, ***(c)*** At $f = 1$ kHz



a *b* *c* *d*

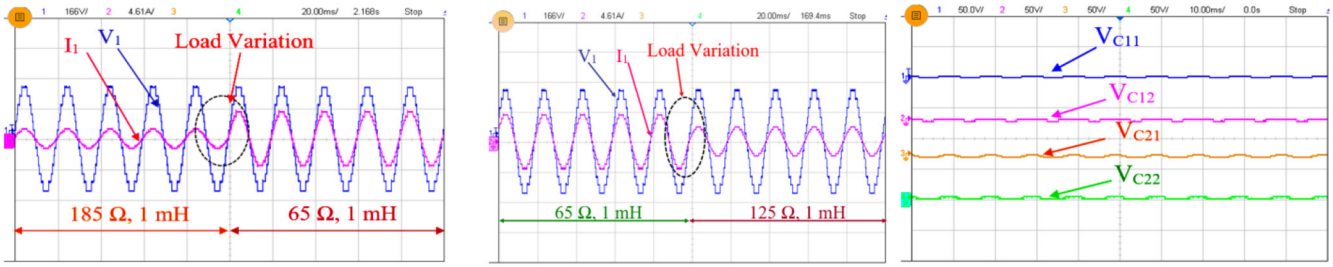
Fig. 16 *Simulation waveforms of the proposed 13L-SCMLI (H)*

(a) Output voltage (V_1) and current (I_1) waveform at $f = 50$ Hz, ***(b)*** Capacitor output voltage waveform (V_{c11}, V_{c21}, V_{c21} and V_{c22}) at $f = 50$ Hz, ***(c)*** Output voltage (V'_1) and current (I'_1) waveform at $f = 400$ Hz, ***(d)*** Capacitor output voltage waveform (V'_{c11}, V'_{c21}, V'_{c21} and V'_{c22}) at $f = 400$ Hz

proposed SCMLI under *R–L* (80 Ω–100 mH) load condition is shown in Figs. 15*a* and *b*.

8.2 Results of the proposed 13L-SCMLI

In this section, results of the proposed 13L-SCMLI (HE) are discussed. As shown in Figs. 16*a* and *b*, simulation results representing output voltage, current and voltage across capacitors is shown at $f = 50$ Hz under *R–L* ($R = 65$ Ω, $L = 1$ mH) load condition. Similarly, under the same load condition at $f = 400$ Hz simulation results are shown in Figs. 16*c* and *d*. While, experimental results are shown in Figs. 17*a* and *b* representing the feasibility of the proposed SCMLI under dynamic load variation and output voltage across capacitors is shown in Fig. 17*c* under *R–L* ($R = 65$ Ω, $L = 1$ mH) load at $f = 50$ Hz. In conclusion, the above discussed waveforms represent the operability of the proposed SCMLI under dynamic conditions. The experimental prototype used for testing is shown in Fig. 18. Fig. 19 represents the efficiency graph for the proposed 9L-SCMLI w.r.t. to load variation at $f = 50$ Hz having efficiency up to 97.08% ($R = 225$ Ω, $L = 1$ mH).



a b c

Fig. 17 *Experimental waveforms of the proposed 13L-SCMLI (H). Output voltage (V_1) and current (I_1) waveform having dynamic load variation at $f = 50$ Hz*
(a) Varying from 65 Ω, 1 mH to 125 Ω, 1 mH, ***(b)*** Varying from 185 Ω, 1 mH to 65 Ω, 1 mH, ***(c)*** Capacitor output voltage waveforms (V_{c11}, V_{c21}, V_{c21} and V_{c22})

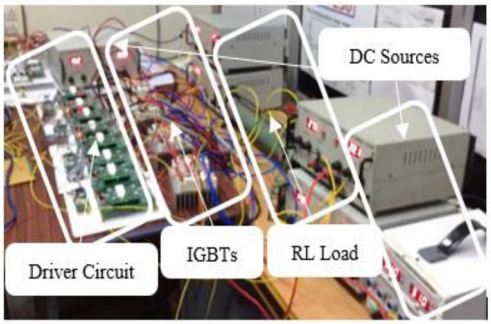


Fig. 18 *Experimental prototype model*

Fig. 19 *Efficiency analysis w.r.t. load variation*

9 Conclusion

In this paper, a SCMLI configuration for high-frequency medium voltage applications is presented. A 5L-SCMLI is proposed considering the basic configuration, which is further extended to 9L operation with a reduced number of active switches having self-voltage boosting and balancing ability. Further, the proposed 9L-SCMLI is extended up to n level being considered as the basic configuration for the extension of the proposed HE and VE. A generalised switching table is provided for the proposed extension. Design of the size of capacitor demonstrated for the proposed 9L-SCMLI. It is observed that the obtained C_{opt} value is quite smaller as compared to other topologies under several operating conditions. Moreover, power loss analysis is carried out considering resistive loading condition. Comparative study with the other proposed SCMLIs is done with in depth analysis considering all possible factors required to access the proposed SCMLI. Simulation and experimental results for dynamic load varying conditions, sudden change in step input and different modulation index for higher frequency are presented. All the presented results confirmed that the proposed SCMLI is suitable for the HF PDS applications (like electric vehicle, motor drives, microgrid, telecommunications, computer applications and space applications) with features of having less weight, reduced complexity and least CF/N_L value.

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